1. A method of manufacturing a semiconductor comprising:

forming an element isolation region in a semiconductor substrate of a first conductivity type to partition an active area in the semiconductor substrate;

forming a semiconductor region of a second conductivity type in the active area;

causing the active area to overlap the element isolation region;

forming an interlayer insulation film on the element isolation region and the active area;

forming an opening to which the element isolation region, the active area, and a boundary therebetween are exposed;

forming a glue layer in the opening; and

forming a conductor electrically connected to the semiconductor region through the glue layer.

2. The method according to claim 1, wherein the semiconductor substrate is silicon, and a step of causing the active area to overlap the element isolation region includes:

exposing a top surface and a side of the active area; and

forming silicon on the top surface and the side of the active area by selective epitaxial growth growing.

3. The method according to claim 1, wherein the semiconductor substrate is silicon, and a step of causing the active area to overlap the element isolation region includes:

exposing a top surface of the active area and forming, in the element isolation region, a hollow to which a side of the active area is exposed; and

burying silicon in the hollow.

4. The method according to claim 1, further comprising:

forming a metal layer at least on the active area after the active area is caused to overlap the element isolation region;

causing the metal layer to react on the active area to form a reaction layer of metal constituting the metal layer and a semiconductor constituting the active area; and

removing an unreacted portion of the metal layer to leave the reaction layer on a surface of the semiconductor region of the second conductivity type formed in the active area.

5. The method according to claim 2, further comprising:

forming a metal layer at least on the active area after the active area is caused to overlap the element isolation region;

causing the metal layer to react on the active area to form a silicide layer; and

removing an unreacted portion of the metal layer to leave the silicide layer on a surface of the semiconductor region of the second conductivity type formed in the active area.

6. The method according to claim 3, further comprising:

forming a metal layer at least on the active area after the active area is caused to overlap the element isolation region;

causing the metal layer to react on the active area to form a silicide layer; and

removing an unreacted portion of the metal layer to leave the silicide layer on a surface of the semiconductor region of the second conductivity type formed in the active area.

7. A method of manufacturing a semiconductor device comprising:

forming an element isolation region in a semiconductor substrate of a first conductivity type to partition an active area in the semiconductor substrate;

forming a semiconductor region of a second conductivity type in the active area;

etching the element isolation region to expose a side of the active area;

forming a metal layer at least on the active area after the side of the active area is exposed;

causing the metal layer to react on the active area to form a reaction layer of metal constituting the metal layer and a semiconductor constituting the active area; and

removing an unreacted portion of the metal layer and leaving the reaction layer on a surface of the semiconductor region of the second conductivity type formed in the active area.

8. The method according to claim 7, wherein the semiconductor substrate is silicon, and the reaction layer is a silicide layer.